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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,179	09/04/2003	George J. Kluth	0180139	6788

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,179	KLUTH ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 7 and 14 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 7 and 14 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1 – 7 and 14 – 20 in the reply filed on November 29, 2004 is acknowledged.

Claims 8 – 13 have been cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

3. Claim **1 – 3, 6, 7, 14 – 16, 19** and **20** are rejected under 35 U.S.C. 102(e) as being anticipated by Shiraiwa et al. (US Patent No. 6,740,605).

4. Regarding claim **1**, Shiraiwa et al. disclose a memory cell structure comprising:

a semiconductor substrate 16 (fig. 9);

a first silicon oxide layer 28 (fig. 9) situated over said semiconductor substrate,

a charge storing layer 30 (fig. 9) situated over said first silicon oxide layer, said charge storing layer comprising silicon nitride having reduced hydrogen content (col. 2 , lines 23 – 28 and 56 – 65), said reduced hydrogen content reducing charge loss in said charge storing layer (Noted: Shiraiwa et al. do not explicitly show reduced hydrogen content reduces charge loss. However, since the ONO structure contains reduced hydrogen content it would reduce charge loss);

a second silicon oxide layer 32 (fig. 9) situated over said charge storing layer;

a gate layer 24 (fig. 9) situated over said second silicon oxide layer.

Regarding claim **2**, Shiraiwa et al. disclose first silicon oxide layer, charge storing layer, second silicon oxide layer, and gate layer forming a gate stack 27 (fig. 9), the gate stack having a sidewall;

a spacer 40 (fig. 9) adjacent to the sidewall of said gate stack, said spacer comprising silicon nitride (col. 13, line 44) having reduced hydrogen content (col. 2 , lines 23 – 28 and 56 – 65), said reduced hydrogen content reducing charge loss in said charge storing layer (Noted: Shiraiwa et al. do not explicitly show reduced hydrogen content reduces charge loss. However, since the ONO structure contains reduced hydrogen content it would reduce charge loss).

Regarding claim **3**, Shiraiwa et al. disclose the gate stack is situated over a channel region 18 (fig. 9) in the semiconductor substrate, said channel region situated between a first terminal region 12 (fig. 9) and a second terminal region 14 (fig. 9).

Regarding claim **6**, Shiraiwa et al. disclose the SONOS device known as dual-bit, two-bit or multi-bit memory (col. 1, lines 43, 65 and 66).

Regarding claim **7**, Shiraiwa et al. disclose the charge storing layer is formed from nitrogen radicals (col. 3, lines 19 – 41).

Regarding claim **14**, Shiraiwa et al. disclose a memory cell structure comprising:

a semiconductor substrate 16 (fig. 9), a first silicon oxide layer 28 (fig. 9) situated over said semiconductor substrate, a charge storing layer 30 (fig. 9) situated over said first silicon oxide layer, a second silicon oxide layer 32 (fig. 9) situated over said charge storing layer; a gate layer 24 (fig. 9) situated over said second silicon oxide layer, said memory structure characterized by:

said charge storing layer comprising silicon nitride having reduced hydrogen content (col. 2 , lines 23 – 28 and 56 – 65): said reduced hydrogen content reducing charge loss in said charge storing layer (Noted: Shiraiwa et al. do not explicitly show reduced hydrogen content reduces charge loss. However, since the ONO structure contains reduced hydrogen content it would reduce charge loss in the charge storing layer).

Regarding claim **15**, Shiraiwa et al. disclose first silicon oxide layer, charge storing layer, second silicon oxide layer, and gate layer forming a gate stack 27 (fig. 9), the gate stack having a sidewall;

a spacer 40 (fig. 9) adjacent to the sidewall of said gate stack, said spacer comprising silicon nitride (col. 13, line 44) having reduced hydrogen content (col. 2 , lines 23 – 28 and 56 – 65), said reduced hydrogen content reducing charge loss in said charge storing layer (Noted: Shiraiwa et al. do not explicitly show reduced hydrogen content reduces charge loss. However, since the ONO structure contains reduced hydrogen content it would reduce charge loss in the charge storing layer).

Regarding claim **16**, Shiraiwa et al. disclose the gate stack is situated over a channel region 18 (fig. 9) in the semiconductor substrate, said channel region situated between a first terminal region 12 (fig. 9) and a second terminal region 14 (fig. 9).

Regarding claim **19**, Shiraiwa et al. disclose the SONOS device known as dual-bit, two-bit or multi-bit memory (col. 1, lines 43, 65 and 66).

Regarding claim **20**, Shiraiwa et al. disclose the charge storing layer is formed from nitrogen radicals (col. 3, lines 19 – 41).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **4, 5, 17 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraiwa et al. (US Patent No. 6,740,605).

7. Regarding claim **4**, Shiraiwa et al. disclose the claimed invention of claim 1 and also show the charge storing layer has a hydrogen content greater than 3 atomic percent (col. 10, lines 62+ and col. 11, lines1 – 20).

Shiraiwa et al. do not explicitly show the charge storing layer has a hydrogen content less than 1.0 atomic percent as cited in current claim.

However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a charge storing layer has a hydrogen content less than 1.0 atomic percent as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Regarding claim **5**, Shiraiwa et al. disclose the claimed invention of claim 1 and also show the charge storing layer has a hydrogen content greater than 3 atomic percent (col. 10, lines 62+ and col. 11, lines1 – 20).

Shiraiwa et al. do not explicitly show the charge storing layer has a hydrogen content between 0 and 0.5 atomic percent as cited in current claim.

However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a charge storing layer has a hydrogen content between 0 and 0.5 atomic percent as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Regarding claim **17**, Shiraiwa et al. disclose the claimed invention of claim 14 and also show the charge storing layer has a hydrogen content greater than 3 atomic percent (col. 10, lines 62+ and col. 11, lines1 – 20).

Shiraiwa et al. do not explicitly show the charge storing layer has a hydrogen content less than 1.0 atomic percent as cited in current claim.

However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a charge storing layer has a hydrogen content less than 1.0 atomic percent as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Regarding claim **18**, Shiraiwa et al. disclose the claimed invention of claim 14 and also show the charge storing layer has a hydrogen content greater than 3 atomic percent (col. 10, lines 62+ and col. 11, lines1 – 20).

Shiraiwa et al. do not explicitly show the charge storing layer has a hydrogen content between 0 and 0.5 atomic percent as cited in current claim.

However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a charge storing layer has a hydrogen content

between 0 and 0.5 atomic percent as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

January 18, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800